ABSTRACT OF THE DISCLOSURE

Adjustment circuitry in a phase-locked loop (PLL) adjusts a sampling point to any desired location within a bit period of each bit of received high-speed serial data. The adjustment circuitry, responsive to program control, selectively adds current portions to a charge pump error current output thereby adjusting a feedback signal frequency to shift the serial data sampling point. A plurality of current mirror devices is scaled, with respect to a reference current device, to provide ΔI current portions. A current control module controls the current portions magnitude and a sign of the current portions. The adjustment circuitry further controls charge pump programmable current sources in order to set a desired operating point of the PLL. The programmable current sources are controlled by a bias voltage and a plurality of selectable serial and parallel coupled resistors.